UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/088,913	05/07/2002	Michael O. Thompson	0104-0704PUS1	8909

2292 7590 12/26/2008

BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER
HUR, JUNG H

ART UNIT	PAPER NUMBER
2824	

NOTIFICATION DATE	DELIVERY MODE
12/26/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/088,913
Filing Date: May 07, 2002
Appellant(s): THOMPSON ET AL.

Michael Mutter
For Appellant

EXAMINER'S ANSWER

This is in response to the supplemental appeal brief filed 14 October 2008 and the appeal brief filed 24 June 2008 appealing from the Office action mailed 08 January 2008.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is deficient. 37 CFR 41.37(c)(1)(v) requires the summary of claimed subject matter to include: (1) a concise explanation of the subject matter defined in each of the independent claims involved in the appeal, referring to the specification by page and line number, and to the drawing, if any, by reference characters and (2) for each independent claim involved in the appeal and for each dependent claim argued separately, every means plus function and step plus function as permitted by 35 U.S.C. 112, sixth paragraph, must be identified and the structure, material, or acts described in the specification as corresponding to each claimed function must be set forth with reference to the specification by page and line number, and to the drawing, if any, by reference characters.

The brief is deficient because:

Throughout the Summary, Appellant refers to the reference characters S_1 - S_q as bit lines; however, in Figs. 5 and 6 of Appellant's disclosure, the bit lines are designated with the reference characters BL's (for example, BL_1 - BL_k), while the reference characters S_1 - S_q represent segments.

Further, at the end of the first paragraph in the Summary, Appellant states that "[a] passive memory requires each memory cell be at all times in physical ohmic contact with a word line and a bit line" (emphasis added). This highlighted feature is not claimed and not supported in the cited portion of the specification, namely, page 7, line 8 through page 9, line 35.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,487,029	Kuroda	1-1996
4,599,709	Clemons	7-1986
5,734,615	Dierke	3-1998
5,969,380	Seyyedy	10-1999

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 13, 14, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda (U.S. Pat. No. 5,487,029) in view of Clemons (U.S. Pat. No. 4,599,709).

Regarding claims 1, 13 and 17, Kuroda, for example in Figs. 1 and 2, discloses a non-volatile passive matrix memory device comprising ferroelectric memory cells (for example, C0-C7 in Fig. 2); word lines (for example, W00-W07 in Fig. 2) and bit lines (for example, D0-D7 in Fig. 2) that are orthogonal to each other, where each memory cell is at all times in physical contact with a word line and a bit line (for example, in Fig. 2, the memory cell C0 is directly connected to or is directly contacting the word line W00 and the bit line D0; i.e., a transistor is not used to make a connection or contact to a word line or a bit line); the word lines divided into a number of segments (for example, BLOCK (0,0) through BLOCK (0,7) in Fig. 1), each segment comprising and being defined by a plurality of adjoining bit lines (for example, D0-D7 for BLOCK (1,0)); each word line in a segment is differentiated based on the position of the word line within the segment (i.e., in different row positions), each word line in the segment being adjoined to a separate bit line (i.e., in a matrix structure); a plurality of sensing means (for example, SA in WRC0-WRC7), each being adapted for sensing the charge flow in the bit line

connected therewith in order to determine a logical value stored in the memory cell defined by the bit line (see, for example, column 12, lines 42-54).

However, Kuroda does not disclose means for connecting each separate bit line assigned to a segment with a different associated sensing means, such that a world line of the same position within each segment is selected within each segment, each word line of the same position being sensed at the same time by said respective different associated sensing means, thus enabling simultaneous connection of all memory cells assigned to a word line on a segment for readout via the corresponding bit lines of the segment.

Clemons, for example in Figs. 2 and 3, discloses a means (for example, via T200-T203 controlled by BYTE BLOCK DECODER) for connecting each separate bit line (for example, bit lines for columns C11-C14) assigned to a segment (for example, BYTE BLOCK 1, when selected) with a different associated sensing means (for example, SA1-SA4 via I/O SWITCHES in Fig. 3), such that the world line of the same position within each segment is selected within each segment (i.e., for example, a selected word line within BYTE BLOCK 1), each word line of the same position being sensed at the same time by said respective different associated sensing means (for example, SA1-SA4 via I/O SWITCHES in Fig. 3), thus enabling simultaneous connection of all memory cells (for example, M111 - M114) assigned to a word line (for example, R1) on a segment (for example, BYTE BLOCK 1) for readout via the corresponding bit lines (for example, bit lines for columns C11 - C14) of the segment.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify the device of Kuroda by incorporating the means of Clemons for connecting each bit line assigned to a segment with an associated sensing

means, thus enabling simultaneous connection of all memory cells assigned to a word line on a segment for readout via the corresponding bit lines of the segment, as an equivalent alternative means for segmenting and simultaneously accessing a byte (or a word or other widths of bits) of information from the memory (compare with Fig. 1 of Clemons, which is similar to the configuration of Kuroda), for the purpose of having a ferroelectric memory organization that provides for improved utilization of spare columns, while allowing for subdivision of the memory into portions (see Clemons column 3, lines 40-43).

Regarding claims 14 and 16, the above Kuroda/Clemons combination further discloses that the number of sensing means is equal to the number of bit lines within each segment (for example, Figs. 2 and 3 of Clemons, as applied to the above combination, show 4 sensing means SA1-SA4 for 4 bit lines within each segment or BYTE BLOCK), where each segment contains the same number of bit lines (for example, 4 bit lines in each BYTE BLOCK in Fig. 2 of Clemons), such that each bit line in each segment (when selected) is sensed at a different sensing means (via corresponding SA1-SA4 in Fig. 3 of Clemons).

Claims 2-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda (U.S. Pat. No. 5,487,029) in view of Clemons (U.S. Pat. No. 4,599,709) as applied to claim 1 above, and further in view of Dierke (U.S. Pat. No. 5,734,615).

Regarding claim 2, the combination of Kuroda and Clemons discloses a non-volatile passive matrix memory device as in claim 1 above, with the exception of the

simultaneous connection of each bit line of a segment with the associated sensing means during addressing is accomplished by multiplexers.

Dierke, for example in Fig. 7, discloses multiplexers (42-0' through 42-7') for simultaneously connecting (since multiplexers are commonly controlled) each bit line of a segment (three segments defined by BIT 0-7, BIT 8-15 and BIT 16-23) with an associated sensing means (at the output of each multiplexer).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to substitute the multiplexing means of Dierke for the multiplexing means of Clemons, since both means are equivalent for simultaneously connecting bit lines of a segment with an associated sensing means, for the purpose of having a ferroelectric memory organization that provides for improved utilization of spare columns, while allowing for subdivision of the memory into portions (see Clemons column 3, lines 40-43), and the selection of these equivalents would be within the level of ordinary skill in the art.

Regarding claims 3-5, the above Kuroda/Clemons/Dierke combination further discloses that the number of multiplexers corresponds to the largest number of bit lines defining a segment (in Fig. 7 of Dierke, eight bit lines per segment; when adapted for Clemons with four multiplexers; see Clemons, Fig. 2), each bit line of a segment being connected with a 3 multiplexer (see Dierke, Fig. 7 in which BIT 0-7, for example, are connected to the respective multiplexers); wherein the output of each multiplexer is connected with a signal sensing means (inherent in Dierke, Fig. 7; SA1-SA4 in Fig. 3 of

Clemons); wherein the signal sensing means is a sense amplifier (SA1-SA4 in Fig. 3 of Clemons).

Claims 12, 15 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda (U.S. Pat. No. 5,487,029) in view of Clemons (U.S. Pat. No. 4,599,709) as applied to claim 1, 14 and 17 above, and further in view of Seyyedy (U.S. Pat. No. 5,969,380).

Regarding claims 12, 15 and 18, the combination of Kuroda and Clemons discloses a non-volatile passive matrix memory device as in claims 1, 14 and 17 above, with the exception of a volumetric data storage apparatus with a plurality of stacked layers, each layer comprising one of said non-volatile passive matrix memory devices. Seyyedy, for example in Figs. 1 and 2, discloses a ferroelectric volumetric data storage apparatus with a plurality of stacked layers (for example, four layers in Fig. 1 and three layers in Fig. 2), each layer comprising one of non-volatile passive matrix memory devices (planar ferroelectric memory arrays). It would have been obvious at the time the invention was made to a person having ordinary skill in the art to stack a plurality of devices (as discloses in the above combination of Kuroda and Clemons) in a volumetric data storage apparatus, as in Seyyedy, for the purpose of increasing the density of memory cells over a given substrate area.

(10) Response to Argument

In responding to Appellant's arguments below, Examiner used the same headings and subheadings in the ARGUMENTS section of the supplemental brief and attempted to address the specific arguments presented under each of the headings and subheadings in the same order.

A. The Rejections Fail to Establish Prima Facie Obviousness of Independent Claims 1, 12 and 13

1. Argument Summary

In response to the general arguments presented under this subheading (on page 8 of the supplemental brief), Examiner asserts that the reasoning provided in support of the rejections of independent claims 1, 12 and 13 under 35 USC 103 does establish *prima facie* obviousness, and that the cited references, when combined/modified as indicated in the rejections, do teach or suggest all of the claim features, particularly a memory device comprising a passive matrix as recited in independent claims 1, 12 and 13. The support for the Examiner's assertions herein will become evident as the specific arguments are addressed below.

2. The Relied Upon References, Kuroda, Clemons and Seyyedy, Do Not Teach All the Claimed Elements Recited in the Independent Claims.

a. Difference Between Passive, Active and Memories

In response to the general arguments presented under this subheading (in the top paragraph on page 9 of the supplemental brief), Examiner asserts that each of Kuroda and Seyyedy does teach a passive matrix comprising ferroelectric memory cells as defined in independent claims 1, 12 and 13, and that, even though Clemons teaches a different type of memory cells than that of Kuroda, Clemons was cited in the rejections as a secondary reference that teaches an improved multiplexing arrangement which is applicable to the memory device of Kuroda with a reasonable expectation of success, such that when combined with Kuroda, the combination would teach a memory device as recited in independent claims 1, 12 and 13. Again, the support for the Examiner's assertions herein will become evident as the specific arguments are addressed below.

Examiner acknowledges Appellant's general summary of the differences between the various types of memories presented under this subheading, including: the differences between a passive matrix-addressable ferroelectric memory and the active matrix-addressable memory (on pages 9-11 of the supplemental brief); the differences between ferroelectric memories and semiconductor memories such as DRAMs and SRAMs (on pages 11-12 of the supplemental brief); and the discussion with reference to the attachments A/1 through D/11 (on pages 12-15 of the supplemental brief).

b. Teachings of Kuroda

In the first paragraph under this subheading, Appellant argues that "a passive matrix memory requires the ferroelectric material of the capacitor be at all the time are in ohmic contact with the metal electrodes" (emphases added) and that "Appellants recite this language explicitly within claims 1, 12 and 13 which is not taught by Kuroda" (emphasis added). However, Examiner notes that this language as highlighted is not explicitly recited within claims 1, 12 and 13 as presented in Appendix A of the supplemental brief and presently being considered.

In the intervening paragraph between pages 15 and 16 of the supplemental brief, Appellant argues that "nowhere does Kuroda teach or suggest that it provides a passive matrix memory...teach characteristics that conform to a passive matrix memory" and that "the stated object in Kuroda is to improve on an active matrix-addressable memory…by reducing the overall voltage disturb, which Kuroda terms the voltage stress…Kuroda provides a true active memory circuit" (emphases added), and, on pages 16-17, further describes Appellant's understanding of a general operation and a disturb coefficient analysis of Kuroda's memory device in comparison with other memory device configurations, as disclosed in Kuroda.

In response, Examiner notes that, although the object of Kuroda is to improve on an active matrix-addressable memory and reduce the overall voltage disturb/stress, Fig. 1 of Kuroda (see Exhibit A below, which is an annotated version of Fig. 1 of Kuroda) shows a memory device comprising memory cells constituting the elements of a passive

matrix where each memory cell is at all times in physical contact with a word line and a bit line, as recited in independent claims 1, 12 and 13 (see lines 8-11 in claim 1, lines 11-14 in claim 12 and similar limitations in lines 7-10 in claim 13 in Appendix A).

Further, in the middle paragraph on page 16, Appellant asserts that Kuroda reduces "the voltage disturb…by selecting a single memory circuit of a block...at a time and then selecting a single memory cell of this memory circuit..." (emphases added), implying that a single memory cell is selected at a time. However, Examiner notes that this characterization of Kuroda's memory device appears to be erroneous. First, Kuroda teaches that data is written/read "at the unit of 8 bits" (see for example column 6, lines 4-5). Second, Fig. 1 of Kuroda (Exhibit A below) shows that, when the decoder YDEC activates one of Y0-Y7, same columns in respective blocks in a row of blocks (for example, BLOCK (1,0) through BLOCK (1,7)) are selected in parallel or simultaneously for readout, since Y0-Y7 extend across all the Y-SELECT circuits in the multiplexing arrangment. For example, in Exhibit A above, the Y0 signal selects in parallel or simultaneously the first columns in the respective blocks in a row of blocks. Therefore, Kuroda's memory device does not select a single memory cell at a time, as implied by Appellant, but rather is intrinsically configured to readout in parallel or simultaneously.

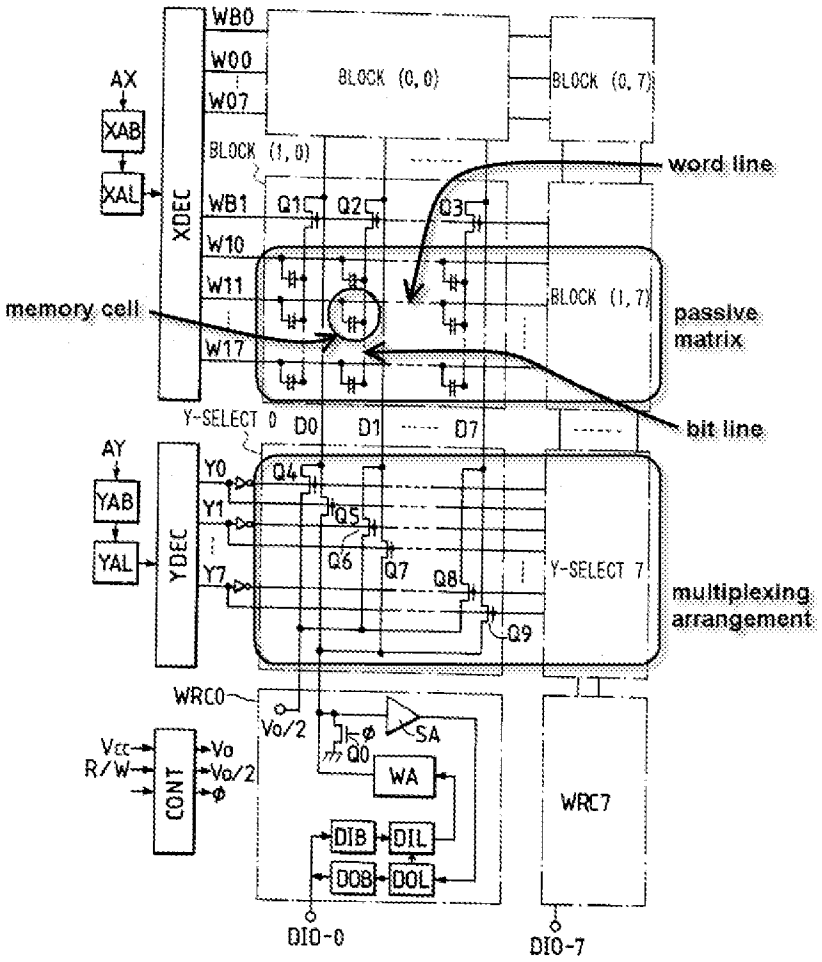


Exhibit A
(Kuroda, Fig. 1)

c. Teachings of Clemons

Under this subheading, Appellant argues that "Clemons concerns a completely different kind of memory…and a multi-bit organization" and that "Clemons teaches nothing more than providing a bytewise-organized memory...such that, for instance, a byte may be read in parallel from one row of memory cells in a block at a time" (emphasis added).

In response, Examiner notes that, even though Clemons concerns a different kind of memory than that of Kuroda, Clemons' multi-bit organization or bytewise-organization of the memory, achieved with an improved multiplexing arrangement (see Exhibit B below, which is an annotated version of Fig. 2 of Clemons), is applicable to other kinds of memory including that of Kuroda, since both kinds of memory use word lines, bit lines and a multiplexing arrangement to select and access desired memory cells (see Exhibits A and B).

Further, Clemons' multi-bit organization or bytewise-organization of the memory, achieved with an improved multiplexing arrangement (see Exhibit B below), is precisely the reason Examiner cited Clemons in the rejections, to provide the benefits and advantages of such memory organization (or multiplexing arrangement) for the memory of Kuroda.

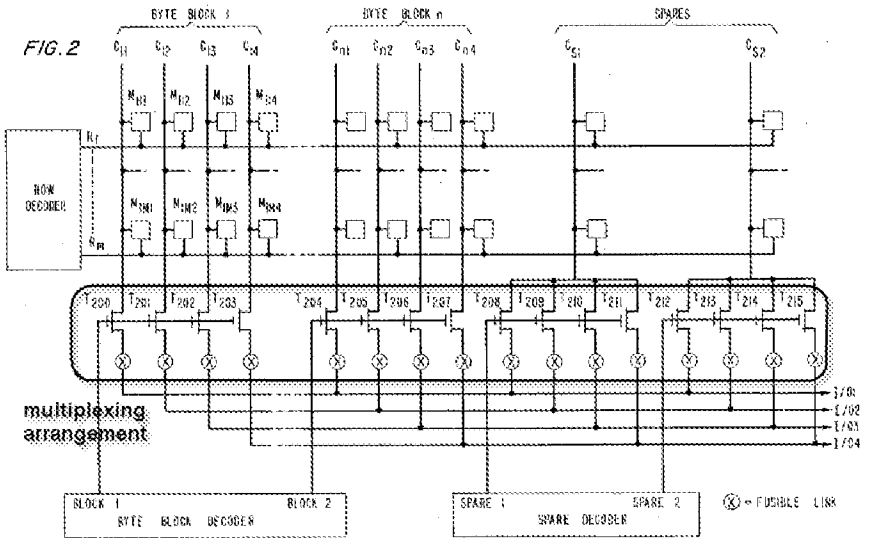


Exhibit B
(Clemons)

3. One of Ordinary Skill Would Not Combine the Teachings of Clemons with Kuroda to Achieve Appellants Claimed Invention

a. Kuroda Does Not Teach or Suggest Parallel Read Out- One of Ordinary and of Common Sense in the Art Would Not Conclude it Obvious to Try to Force Parallel Readout on Kuroda's Memory by Combining it with Clemons Teachings

In response to Appellant's argument (in the middle paragraph on page 18) that "Kuroda does not allow for parallel readout" (emphases added) and that "[o]nly a single memory cell of a single circuit in one block of a column of blocks is read at a time" (emphases added), Examiner notes that this characterization of Kuroda appears to be erroneous, as noted previously. First, Kuroda teaches that data is written/read "at the unit of 8 bits" (see for example column 6, lines 4-5). Second, Fig. 1 of Kuroda (Exhibit A above) shows that, when the decoder YDEC activates one of Y0-Y7, same columns in the respective blocks in a row of blocks (for example, BLOCK (1,0) through BLOCK (1,7)) are selected in parallel or simultaneously for readout, since Y0-Y7 extend across all the Y-SELECT circuits in the multiplexing arrangment.

In the same paragraph, Appellant states that "in principle of course a parallel read could be obtained in Kuroda by allowing in the simultaneous reading of one memory cell in each block…" (emphases added), implying that the simultaneous reading can be optionally selected. However, a parallel readout is not optional in Fig. 1 of Kuroda but rather intrinsic, as noted above.

Further, in the same paragraph, Appellant further argues that "[a]ttempting parallel readout in this manner would *increase* the disturb coefficient by a factor of 8" (emphasis added by Appellant). It appears that this argument is based on Appellant's erroneous characterization of Kuroda's device that only a single memory cell is read at a time. Therefore, this argument is moot since Kuroda's memory device is intrinsically configured to readout in parallel or simultaneously.

In response to Appellant's argument, in the bottom paragraph on page 18, that "Kuroda discloses essentially a very small memory capable of storing only 1024 bits", Examiner notes that the number of bits or the size of the memory is not explicitly claimed.

In the top paragraph on page 19, Appellant's statements of Kuroda having "namely, an access rate of one bit at a time from each memory…" (emphasis added) and "if one attempts to modify Kuroda with multiplexing arrangements for parallel readout…" (emphasis added) again indicates Appellant's erroneous characterization of Kuroda's memory device. As noted previously, Kuroda teaches that data is written/read "at the unit of 8 bits" (see for example column 6, lines 4-5), and Fig. 1 of Kuroda (Exhibit A above) shows that, when the decoder YDEC activates one of Y0-Y7, same columns in the respective blocks of a row of blocks (for example, BLOCK (1,0) through BLOCK (1,7)) are selected in parallel or simultaneously for readout, since Y0-Y7 extend across all the Y-SELECT circuits in the multiplexing arrangment. Therefore, Kuroda does not require any modification in order to readout in parallel or simultaneously.

Further, at the end of the same paragraph, Appellant argues that "the proposed hypothetical memory circuit with the multiplexing arrangement of Clemons would have an increased voltage disturb coefficient and lowered reliability" (emphases added). Again, it appears that this argument is based on Appellant's erroneous characterization of Kuroda's device that only a single memory cell is read at a time, while Clemons' multiplexing arrangment adapted for Kuroda's memory yields a bytewise parallel read and write. As noted previously, Kuroda teaches that data is written/read "at the unit of 8 bits" (see for example column 6, lines 4-5), and Fig. 1 of Kuroda (Exhibit A above) shows that, when the decoder YDEC activates one of Y0-Y7, same columns in the respective blocks of a row of blocks (for example, BLOCK (1,0) through BLOCK (1,7)) are selected in parallel or simultaneously for readout, since Y0-Y7 extend across all the Y-SELECT circuits in the multiplexing arrangment. Therefore, this argument is moot since Kuroda's memory device is intrinsically configured to readout in parallel or simultaneously and, when modified with the multiplexing arrangement of Clemons, would not increase the voltage disturb coefficient.

In the bottom paragraph on page 19, Appellant states that "the prior art ferroelectric memory of Kuroda might be modified by the multiplexer arrangement of Clemons to yield a bytewise parallel read and write" (emphasis added), thus admitting that, at least structurally, the multiplexing arrangement of Clemons is applicable to the memory device of Kuroda.

However, in the same paragraph, Appellant further states that such modification would end up "with an eightfold increased voltage disturb coefficient" (emphasis added).

Again, it appears that this argument is based on Appellant's erroneous characterization of Kuroda's device that only a single memory cell is read at a time, while Clemons' multiplexing arrangment adapted for Kuroda's memory yields a bytewise parallel read and write. However, as noted previously, Kuroda teaches that data is written/read "at the unit of 8 bits" (see for example column 6, lines 4-5), and Fig. 1 of Kuroda (Exhibit A above) shows that, when the decoder YDEC activates one of Y0-Y7, same columns in the respective blocks of a row of blocks (for example, BLOCK (1,0) through BLOCK (1,7)) are selected in parallel or simultaneously for readout, since Y0-Y7 extend across all the Y-SELECT circuits in the multiplexing arrangment. Therefore, this argument is moot since Kuroda's memory device is intrinsically configured to readout in parallel or simultaneously and, when modified with the multiplexing arrangement of Clemons, would not increase the voltage disturb coefficient.

In the top paragraph on page 20, Appellant argues that "[t]he teaching of Clemons would actually ruin the expressed object of Kuroda…would increase the voltage stress ratio of Kuroda's memory eightfold...would also serve to make Kuroda's memory rather more complicated...cannot be adapted to a memory of Kuroda" (emphases added).

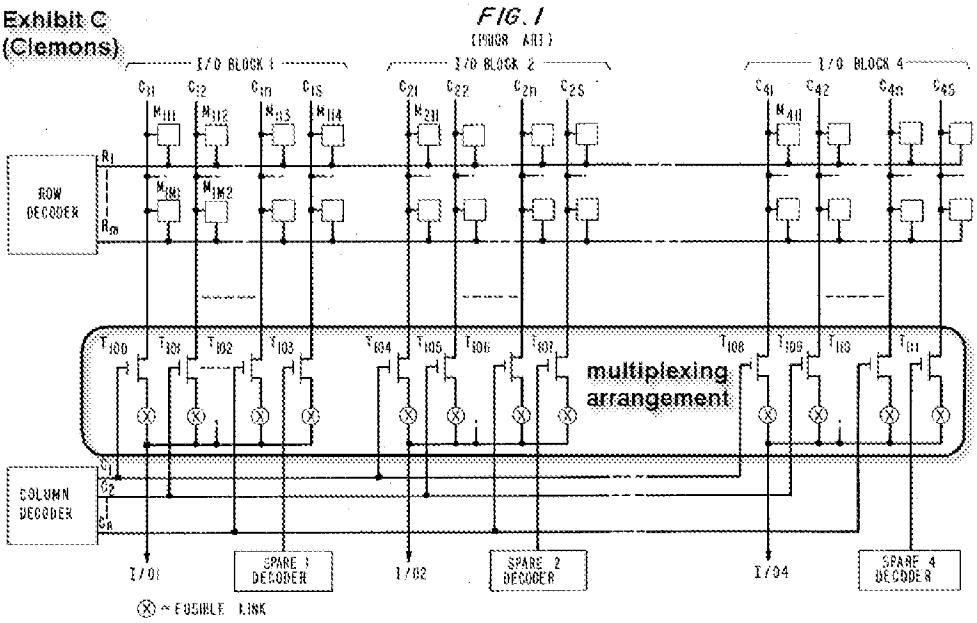
First, it appears that this argument is based on Appellant's erroneous characterization of Kuroda's device that only a single memory cell is read at a time, while Clemons' multiplexing arrangment adapted for Kuroda's memory yields a bytewise parallel read and write. As noted above, Kuroda teaches that data is written/read "at the unit of 8 bits" (see for example column 6, lines 4-5), and Fig. 1 of Kuroda (Exhibit A above) shows that, when the decoder YDEC activates one of Y0-Y7, same columns in the

respective blocks of a row of blocks (for example, BLOCK (1,0) through BLOCK (1,7)) are selected in parallel or simultaneously for readout, since Y0-Y7 extend across all the Y-SELECT circuits in the multiplexing arrangment. Therefore, the argument that Clemons' teaching would increase "the voltage stress ratio" is moot since Kuroda's memory device is intrinsically configured to readout in parallel or simultaneously and, when modified with the multiplexing arrangement of Clemons would not increase the voltage stress ratio.

Further, adapting Clemons' multiplexing arrangment to Kuroda's memory does not necessarily make Kuroda's memory more complicated, since it simply requires that the transistors in the Y-SELECT circuits in Fig. 1 of Kuroda be rearranged into a multiplexing arrangement similar to that shown in Fig. 2 of Clemons (see Exhibit B above), while the number of sense amplifiers would remain the same.

Note that the multiplexing arrangement of Clemons' prior art Fig. 1 (Exhibit C below) is essentially same as the multiplexing arrangment in Fig. 1 of Kuroda (Exhibit A above), i.e., same columns from respective blocks are selected in parallel or simultaneously (for example, in Exhibit C below, the C1 signal selects the first columns in the respective blocks in parallel or simultaneously). Therefore, since Clemons' multiplexing arrangement in Fig. 2 is disclosed as an improvement over the prior art multiplexing arrangement, one of ordinary skill in the art would be motivated to modify the multiplexing arrangement of Kuroda in a similar manner as taught in Clemons.

Exhibit C
(Clemons)



In summary, Examiner has shown that the reasoning provided in support of the rejections of independent claims 1, 12 and 13 under 35 USC 103 does establish *prima facie* obviousness, and that the cited references, when combined/modified as indicated in the rejections, do teach or suggest all of the claim features.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/J. H. Hur/ 12/19/2008

Primary Patent Examiner, Art Unit 2824

Conferees:

J. H. Hur /JH/ 12/19/2008

Richard Elms

/Richard Elms/ /R.T.E./

Supervisory Patent Examiner, Art Unit 2824 12/22/08

Darren Schuberg /D. S./

TQAS TC 2800

/